14nm Educational Design Kit: Capabilities, Deployment and Future

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Abstract— An open Educational Design Kit (EDK) which supports a 14nm FinFET design with all the necessary design rules, models, technology files, verification and extraction command decks, scripts, symbol libraries, and PyCells. It also includes a Digital Standard Cell Library (DSCL); an I/O Standard Cell Library (IOSCL); a set of memories (SOM) with different word and data depths; and a phase-locked loop (PLL). These components of the EDK augment any type of design for educational and research purposes. Though the EDK does not contain any foundry information, it allows 14nm FinFET technology with high accuracy to be implemented in the designs.

Keywords - design kit; low power; pycell.

I. Introduction

In the age of nanometer technologies, universities strive to provide the most modern and high quality studies in IC design. In addition to Electronic Design Automation (EDA) tools from leading companies, Educational Design Kits (EDKs), which include Digital and I/O Standard Cell Libraries for different IC fabrication technologies, are also necessary. But creation of such EDKs is challenged by numerous difficulties such as labor-intensive development and considerable complexity of verification. However, the most important of the challenges are the intellectual property (IP) restrictions imposed by IC fabrication foundries which do not allow universities to copy their technology into EDKs. That is why it became necessary for Synopsys to create an EDK which on one hand did not contain confidential information from foundries, and on the other hand, had the characteristics very close to the real design kits of the foundries.

II. Overview Of The Libraries

Synopsys has created 14nm FinFET Educational Design Kit (EDK) which is free from intellectual property restrictions and is targeted for educational and research purposes. It is aimed for programs training highly qualified specialists in the sphere of microelectronics at different universities, training facilities, and research centers. The EDK is intended to support the trainees so they can better master today's advanced design methodologies and the capabilities of Synopsys' state-of-the art IC design tools. It allows students to design different ICs using 14nm technology and Synopsys' EDA tools.

The Synopsys EDK contains the following: a technology kit (TK), a Digital Standard Cell Library (DSCL), an I/O Standard Cell Library (IOSCL), an I/O Special Cell Library (IOSpCL), a set of memories (SOM) and a phase-locked loop (PLL).

For the EDK's development, an abstract 14nm FinFET technology was used. While the EDK does not contain actual foundry data, which is confidential information from foundries, it is very close to the real 14nm technology. Using the abstract 14nm technology allowed Synopsys to create an EDK which can be used for study and research of real 14nm design characteristics.

III. Description Of The Technology Kit

The technology kit (TK) is a set of technology files needed to implement the physical aspects of a design. The generic TK for education contains:

A. Design Rules

These rules were created by using the MOSIS Scalable CMOS (SCMOS) design rules [6]. They provide greater portability of designs than if 14nm rules were developed because the sizes in 14nm rules can be larger by 5-20% than those in real foundry processes. An example design rule is illustrated in Figure1.

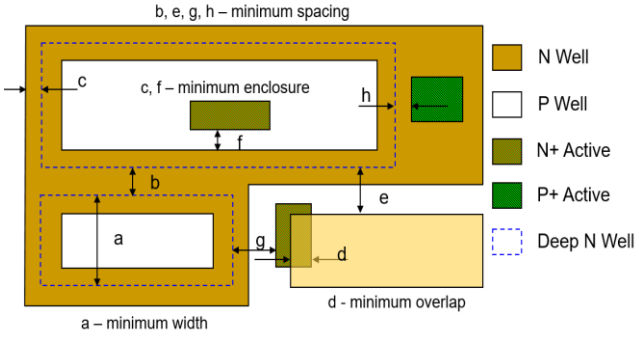

Fig. 1. Example Design Rule

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B. *Device Formation*

This portion of the TK contains the description of available devices and their layout formation rules. It represents all the devices offered in the 14nm 0.8V/1.5V/1.8V generic process.

Figure 2 illustrates examples of device formation.

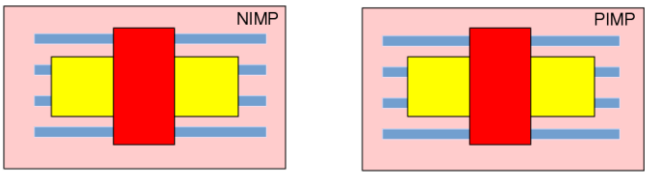

Fig. 2. Examples of Device Formation

C. GDSII Layer Map

This part of the TK contains layer names and GDSII numbers used in the 14nm process. Some layers such as dummy, marking, and text, have been added to the layer map. Any layer numbers may be chosen to form a generic process. A sample of the layer map is shown in Figure 3.

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
1	0	YES	Drawing	FIN	FINi	FINi	FIN
2	0	YES	Drawing	FINCUT	FINCUTi	FINCUTi	FIN cut for printing fine spaces
3	0	YES	Drawing	NWELL	NWELLi	NWELLi	NWELL
4	0	YES	Drawing	DNW	DNWi	DNWi	Deep NWELL
5	0	YES	Drawing	DIFF	DIFFi	DIFFi	Active area, thin oxide for device or interconnection
5	0	YES	Drawing	DDMY	DDMYi	DDMYi	Dummy DIFF layer; must be added if there's DIFF density rule violation
6	0	YES	Drawing	PIMP	PIMPi	PIMPi	P+ source/drain ion implantation
7	0	YES	Drawing	NIMP	NIMPi	NIMPi	N+ source/drain ion implantation
8	0	YES	Drawing	DIFF_15	DIFF_15i	DIFF_15i	1.5v thick oxide (second gate oxide)
9	0	YES	Drawing	DIFF_18	DIFF_15i	DIFF_15i	1.8v thick oxide (second gate oxide)

Fig. 3. Sample of Layer map

D. *Process Description*

This section of the TK provides approximate values of dielectric and metal thicknesses.

E. *Generic SPICE model library*

These are based on the Predictive Technology Model [1]. The SPICE model library contains the following devices:
- transistors,
a) 1.8V devices: thick oxide FinFETs,
b) 1.5V devices: thick oxide FinFETs,
c) 0.8V devices: thin oxide FinFETs with typical, high, and low threshold voltages. Each of these devices have five corner models: TT - both typical; FF - both fast; SS - both slow; SF – slow nfet/fast pfet; FS – slow pfet/fast nfet.
- diode
- rpoly and rmet resistors

In order to estimate the accuracy of the SPICE models, the models' parameters were scaled to 32nm technology to compare them with the characteristics of open 32nm models (Figure 4).

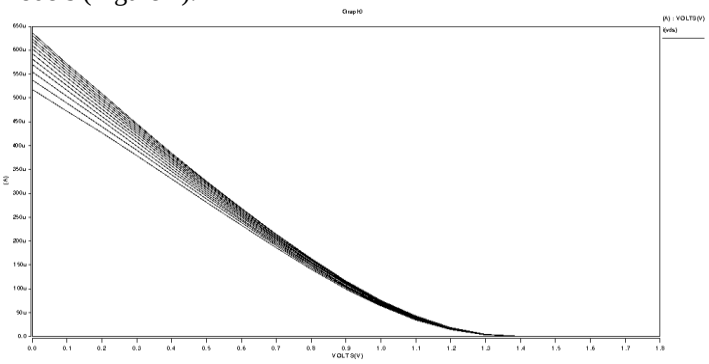

Fig. 4. Bunch of transfer curves for PMOS models

A set of DC transfer curves was obtained and the middle curve from the set was chosen as a typical corner for 1.8V devices, thereby assuring that it is close to the real foundry process. FF, SS, SF and FS corner models were formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%. Figure 5 shows the transfer curves for TT, FF and SS corners of a thin oxide NFET model.

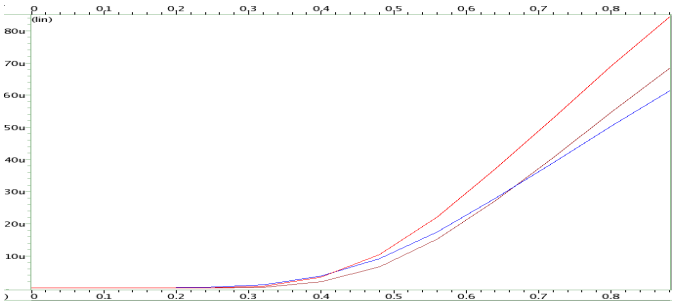

Fig. 5. TT, FF and SS corners of 0.8V Thin oxide High Vth NFET

F. *Milkyway technology file*

This file contains rules used by Synopsys' EDA tools.

G. *OpenAccess[3] symbol library and PyCells*

The OpenAccess symbols and PyCells in this library are: FinFET transistors, resistors, BJTs, and diodes. The PyCells were developed using the Python scripting language complying to PIL 1.1.7 standard to work in any compatible OpenAccess tool, i.e. Synopsys Galaxy™ Custom Compiler.

H. *DRC and LVS rule decks*

These are the design rules needed for Synopsys' IC Validator tools to perform design rule checks and layout vs. schematic.

I. Extraction files

These are files used by the Synopsys StarRC tool for parasitic extraction: ITF, TLU+, mapping, and command files.

J. Support scripts

A variety of additional scripts are required to support the design flow. For example, a script for controlling user input during schematic capture and PyCell setup scripts.

IV. Digital Standard Cell Libraries

The Digital Standard Cell Library (DSCL) is used for designing different ICs in 14nm FinFET technology with Synopsys' EDA tools. The DSCL builds using 1P9M 0.8V/1.5V/1.8V design rules and is aimed at optimizing the main characteristics of an IC design.

The DSCL contains a total of about 1200 cells. The library includes typical combinational logic cells with different drive strengths (inverter, inverting buffer, non-inverting buffer; 2-4 input AND, NAND, OR, NOR cells; 2-3 input XOR, XNOR cells; 2/1-2/2/2 AND-OR, AND-OR-Invert, OR-AND, OR-AND-Invert cells; multiplexers (2 to 1, 3 to 1, 4 to 1); half adder 1-bit and sequential, full adder 1-bit, pos edge DFF (w/ async low-active set, set & reset); neg edge DFF (w/ async active-low set, set & reset, only Q out, only QN out); scan pos edge DFF (w/ async active-low set, reset, set & reset, Q, QN; scan neg edge DFF(w/ async active-low set, reset), multibit DFFs, multibit scan DFFs, TAP cells, Synchronizers, ECO cells and Miscellaneous Cells.

The library also contains all the cells which are required for different styles of low power designs [2]. These cells enable the design of ICs with different core voltages to minimize dynamic and leakage power (clock gating cell, non-inverting delay line; pass gate; hold 0 isolation cell - logic AND; hold 1 isolation cell - logic OR and NOR type of isolation cell); high-to-low level shifter; pos edge retention DFF w/ async active-low clear; always on inverter; always on non-inverting buffer; always on high-to-low level shivter).

Composite Current Source (CCS) modeling technology is used for cell characterization to meet the requirements of contemporary low power design methods. CCS provides timing, noise, and power analyses s while considering the relevant nanometer dependencies. CCS allows the requirements of variation-aware analysis to be met.

In order to fully meet the requirements of low power design techniques, the DSCL characterizes for the 18 process/voltage/temperature (PVT) conditions (Table 1) as well as additional PVT conditions is used to characterize level-shifter cells.

TABLE I
Characterization Conditions

Normal Voltage Operating Condition	
Corner	PVT
tt0p8v25c	Typical/0.8/25^{0}c
tt0p8v125c	Typical/0.8/125^{0}c
tt0p8vm40c	Typical/0.8/-40^{0}c
ss0p72v25c	Slow/0.72/25^{0}c
ss0p72v125c	Slow/0.72/125^{0}c
ss0p72vm40c	Slow/0.72/-40^{0}c
ff0p88v25c	Fast/0.88/25^{0}c
ff0p88v125c	Fast/0.88/125^{0}c
ff0p88vm40c	Fast/0.88/-40^{0}c
Low Voltage Operating Condition	
tt0p6v25c	Typical/0.6/25^{0}c
tt0p6v25c	Typical/0.6/125^{0}c
tt0p6v25c	Typical/0.6/-40^{0}c
ss0p6v25c	Slow/0.6/25^{0}c
ss0p6v125c	Slow/0.6/125^{0}c
ss0p6vm40c	Slow/0.6/-40^{0}c
ff0p7v25c	Fast/0.7/25^{0}c
ff0p7v125c	Fast/0.7/125^{0}c
ff0p7vm40c	Fast/0.7/-40^{0}c

The DSCL has all the necessary deliverables: databook/user guide; layer usage file (.doc, .txt); symbols (.sdb, .slib); synthesis files (.db, .lib); Verilog simulation models (.v); HSPICE netlists (.sp); extracted RC netlists for (.spf); GDSII layout views (.gds); report files (.drc, .lvs); LEF files (.lef); FRAM views, layout views and runset files (.fram, .cel).

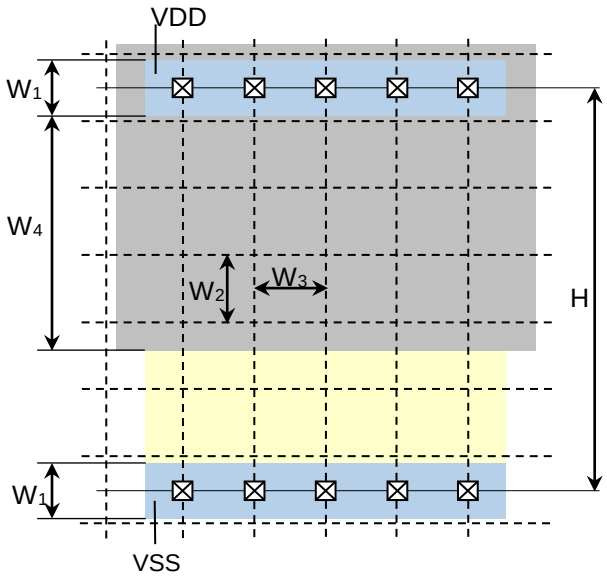

Fig. 6. Physical structure of single height cells

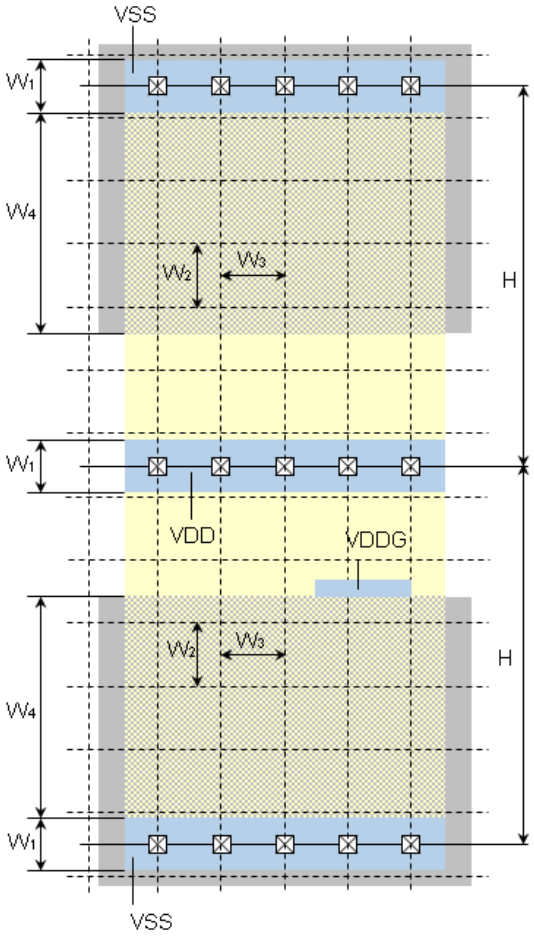

Fig. 7. Physical structure of double height cells

The selection of the physical structures (Figure 6, 7) of the digital cells was made to provide maximum cell density in digital designs as well as to take into consideration the requirements of low power design techniques.

Parameter	Symbol	Value
Cell height	H	0.6
Power rail width	W_1	0.094
Vertical grid	W_2	0.074
Horizontal grid	W_3	0.074
NWell height	W_4	0.3

V. I/O Cell Library

The I/O Standard Cell Library (IOSCL) is used for designing different integrated circuits (ICs) in 14nm technology using Synopsys' EDA tools. It was built using 14nm 1P9M 0.8V/1.5V/1.8V design rules.

Providing a complete set of standard functions, the IOSCL contains 50 cells (including FinFET non-inverting input buffer; FinFET non-inverting bi-directional cell; 4/8/12/16 mA tri-state driver with pull-up and pull-down; analog, non-inverting bidirectional without resistor pad with ESD protection; core power; I/O power; core ground; I/O ground pads; crosscoupling diode; IOVSS to VSS; decoupling capacitors VDD to VSS and IOVDD to IOVSS; break cell; corner pad; filler cell; bonding pad). CCS modeling technology was used for characterization of the IOSCL. All cells are available in wirebond and flip-chip variants with 25um x 200um in size, and all cells are available in EW (East-West) and NS(North-South) variants. for Flip-chip IC design library contains also bump cell for creating flip-chip array(Figure 8).

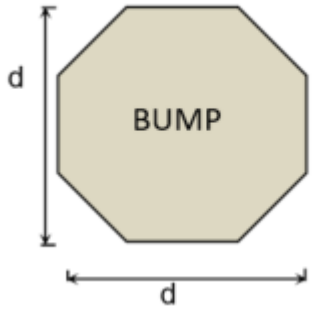

Fig. 8. Physical structure of bump cells for flip-chip array.

The I/O Special Cell Library (IOSpCL) is built using 14nm 1P9M 0.8V/1.5V/1.8V design rules with the same sized as standard I/O cells. The library includes I/Os complying to HSTL[4] and SSTL[5] standards.

CONCLUSION

An Educational Design Kit (EDK) was created and tested by Synopsys. It can be used for educational and research purposes, is free from intellectual property restrictions, and is representative of industrial design kits. It can be used in a wide range of design flows for digital, analog and mixed-signal designs using Synopsys' EDA tools.

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